HYBRID INVERTER FOR WITH ASSOCIATION OF A FIVE LEVEL INVERTER AND A THREE LEVEL TWO SWITCH INVERTER

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Resumo. This paper presents the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multicell with separate dc sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed. This paper also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space-vector modulation. The voltage regulation is obtained by means of a switched power stage, composed of two current sources used to modulate the desired RMS value and waveform in the output stage. Mathematical analysis, experimental and simulation results are presented.

Palavras-chave: *Inverter Multipulse, Hybrid Inverte*

1. INTRODUCTION

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor, while the three-level inverter generates three voltages, and so on.
Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [1]-[3].
The term multilevel starts with the three-level inverter introduced [4]. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems.
Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped) [4]; capacitor-clamped (flying capacitors) [5], [6], [7]; and cascaded multicell with separate dc sources [5], [6], [8]-[10]. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM).
The most attractive features of multilevel inverters are as follows.
1) They can generate output voltages with extremely low distortion and lower dv/dt.
2) They draw input current with very low distortion.
3) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated [8].
4) They can operate with a lower switching frequency.
The results of a patent search show that multilevel inverter circuits have been around for more than 25 years. An early traceable patent appeared in 1975 [9], in which the cascade inverter was first defined with a format that connects separately dc-sourced full-bridge cells in series to synthesize a staircase ac output voltage. Through manipulation of the cascade inverter, with diodes blocking the sources, the diode-clamped multilevel inverter was then derived [10].
The diode-clamped inverter was also called the neutral-point clamped (NPC) inverter when it was first used in a three-level inverter in which the mid-voltage level was defined as the neutral point. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, the circuit topology prevailed in the 1980s.

2. INVERTER TOPOLOGIES

A- Capacitor-Clamped Inverter
Fig. 1 illustrates the fundamental building block of a phase-leg capacitor-clamped inverter. The circuit has been called the flying capacitor inverter [5], [6], [7] with independent capacitors clamping the device voltage to one capacitor voltage level. The inverter in Fig. 3(a) provides a three-level output across a and n, i.e., $V_{an}=V_{dc}/2$, 0, or $-V_{an}=V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{an}=V_{dc}/2$, switches S_1' and S_2' need to be turned on; and for the 0 level, either pair (S_1, S_1') or (S_2, S_2') needs to be turned on. Clamping capacitor C_1 is

charged when S_1 and S_1' are turned on, and is discharged when S_2 and S_2'are turned on. The charge of can be balanced by proper selection of the 0-level switch combination.

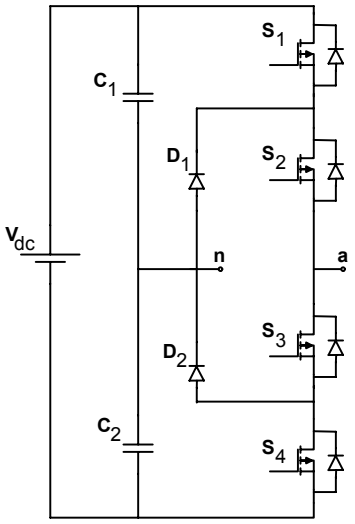

Fig. 1 – Three level capacitor clamped multilevel inverter.

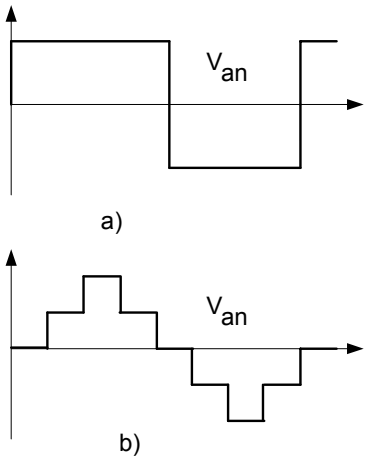

Fig. 2 – Voltage waveform: a) three level; b) five level.

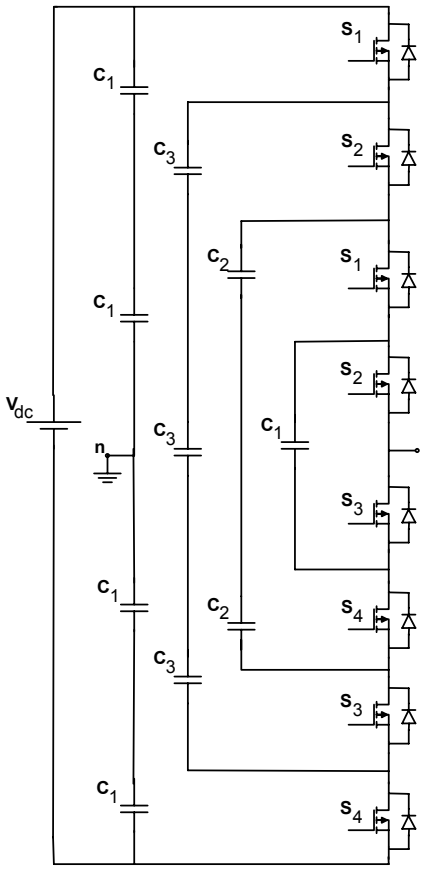

Fig. 3 - Five level capacitor clamped multilevel inverter.

The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Fig. 3 as the example, the voltage of the five-level phase-leg a output with respect to the neutral point n, V_{an}, can be synthesized by the following switch combinations, as showed in Fig. 2 the voltages waveforms for three level inverter and five level inverter.

1) For voltage level $V_{an}=V_{dc}/2$, turn on all upper switches
S_1–S_4.

2) For voltage level $V_{an}=V_{dc}/4$, there are three combinations:
S_1, S_2, S_3, S_1' ($V_{an}=V_{dc}/2$ of upper C_4's -$V_{dc}/4$ of C_1);
S_2, S_3, S_4, S_4' ($V_{an}=3V_{dc}/4$ of upper C_3's -$V_{dc}/2$ of C_4)
S_1, S_3, S_4, S_4' ($V_{an}=V_{dc}/2$ of upper C_4's -$3V_{dc}/4$ of C_3'+$V_{dc}/2$ of C_2's).

3) For voltage level $V_{an}=0$, there are six combinations:
S_1, S_2, S_1', S_2' ($V_{an}=V_{dc}/2$ of upper C_4's -$V_{dc}/2$ of C_2's);
S_3, S_4, S_3', S_4' ($V_{an}=V_{dc}/2$ of upper C_2 -$V_{dc}/2$ of lower C_4);
S_1, S_3, S_1', S_3' ($V_{an}=V_{dc}/2$ of upper C_4's -$3V_{dc}/4$ of C_3's+ $V_{dc}/2$ of C_2's-$V_{dc}/4$ of C_1);
S_1, S_4, S_2', S_3' ($V_{an}=V_{dc}/2$ of upper C_4's -$3V_{dc}/4$ of C_3's+ $V_{dc}/2$ -$V_{dc}/4$ of C_2's of lower C_4's);
S_2, S_4, S_2', S_4' ($V_{an}=3V_{dc}/4$ -$V_{dc}/2$ of C_2's of upper C_3's -$3V_{dc}/4$ +$V_{dc}/4$ of C_1's of C_3's+ $V_{dc}/2$ of C_2's+$V_{dc}/4$ of C_1);
S_2, S_3, S_1', S_4' ($V_{an}=3V_{dc}/4$ of C_3's -$V_{dc}/4$ of C_1's -$V_{dc}/2$ of C_1's of lower C_4's).

4) For voltage level $V_{an}=-V_{dc}/4$, there are three combinations:
S_1, S_1', S_2', S_3' ($V_{an}=V_{dc}/2$ of upper C_4's -$3V_{dc}/4$ of C_3's);
S_4, S_2', S_3', S_4' ($V_{an}=V_{dc}/4$ of C_1's -$V_{dc}/2$ of lower C_4's);
S_3, S_1', S_3', S_4' ($V_{an}=V_{dc}/2$ of C_2's -$V_{dc}/4$ of C_1's -$V_{dc}/2$ of lower C_4's);

5) For voltage level $V_{an}=-V_{dc}/2$, turn on all lower switches, S_1'– S_4'.

In the preceding description, the capacitors with positive signs are in discharging mode, while those with negative sign are in charging mode. By proper selection of capacitor combinations, it is possible to balance the capacitor charge. Similar to diode clamping, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an -level converter will require a total of clamping capacitors per phase leg in addition to main dc-bus capacitors.

B- Capacitor-Clamped Inverter

The Fig. 4 shows the switched audio amplifier operating as a three level Proposed Three Level Half Bridge Inverter half bridge inverter, where this new DC-AC converter have, like output, a sinusoidal voltage with 127V AC RMS, with a frequency of 60 Hz.

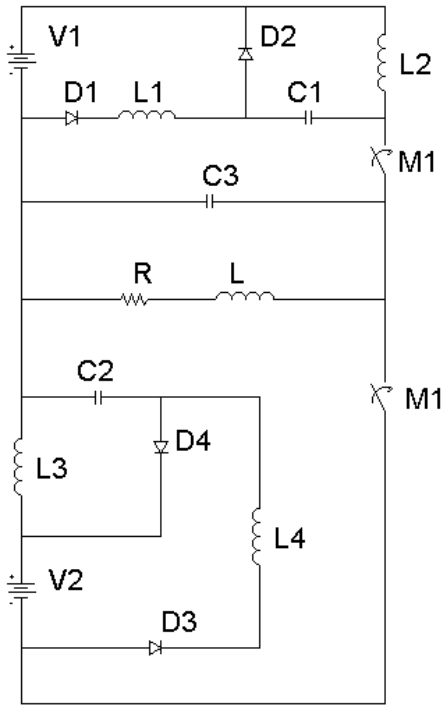

Fig. 4 – Half proposed bridge inverter.

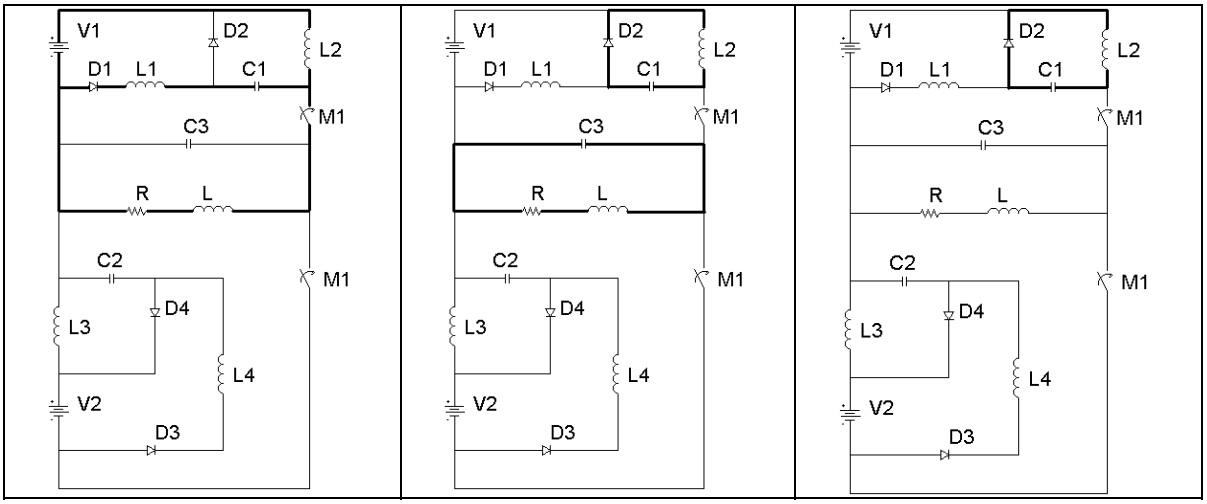

Fig. 5 - Operating stages.

The Proposed Three Level Half Bridge Inverter has the circuit operation for the cases of ILoad>0 and ILoad<0 are symmetrical. The operational principle is summarized referring to the ILoad>0 with waveforms as shown in Fig. 4.
1st STAGE (t0,t1): This stage begins at instant t0, where switch M1 turns on and the resonant inductor changes linearly. During this stage, capacitor C1 discharge occurs which is limited by inductor L1.
2nd STAGE (t1,t2): This stage begins when switch M1 is turned off. This is the freewheeling stage for the inductor L2, where the current flows through diode D2 and the voltage on the load remains clamped by the filter capacitor C3.
3rd STAGE (t2,t3): This stage begins when filter capacitor C3 discharges completely, when the freewheeling remains between inductor L2 and diode D2.
The other cell (M2) analysis is the same.

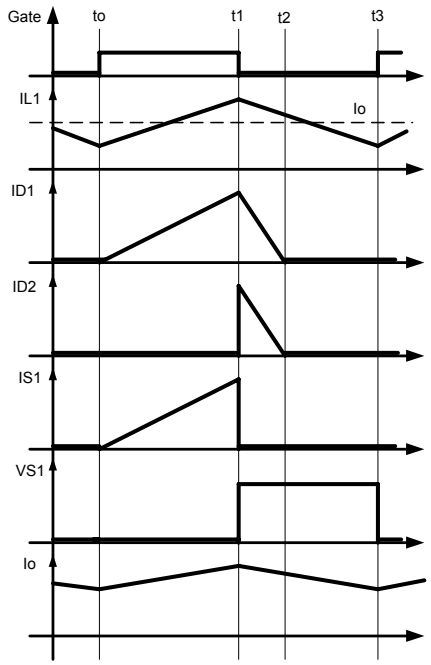

Fig. 6 - The circuit operational waveforms.

If all the elements of the circuit are considered as ideal, it can be assumed that the input power is equal the output power, as in (1):

$$V_{CC1} . I_i = V_C . I_O \tag{1}$$

Where Io is the sum of the currents in the capacitor and the load.

The output current Io is equal to the product between the inductor current and the duty cycle of the switches accreting to the Fig. 4.it is:

$$I_O = D . I_L \tag{2}$$

Analogously, the input current Ii is equal to the output current Io, when the switches are on, except for the current that flows through the diodes when the switches are turned off. Where, it can be written:

$$I_i = D . I_L - (1 - D) . I_L \tag{3}$$

$$I_i = (2 . D - 1) . I_L \tag{4}$$

Substituting (2) and (4) in (1), it gives:

$$\frac{V_i}{V_o} = \frac{(2 \ . \ D \ - \ 1)}{D} \tag{5}$$

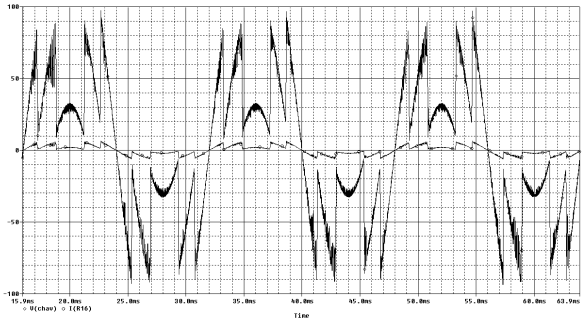

Fig. 7 - Voltage output and current output.

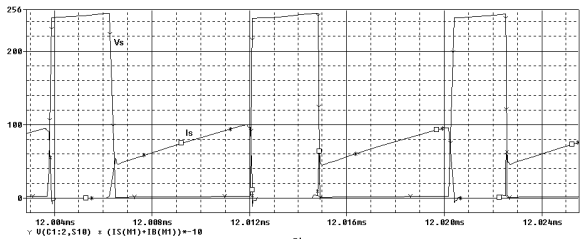

Fig. 8 - Voltage and current waveforms through the resonant capacitors and inductor.

Even though the multipulse inverter has already been built in laboratory, an experimental prototype of the Three Level Half Bridge Inverter is yet to be fully implemented and associated to the aforementioned topology, constituting the proposed Hybrid Inverter with output AC. Therefore additional experimental results will be presented at the final version of this paper.

3. FUNDAMENTAL PRINCIPLES

The Fig. 3 shows the five level capacitor clamped multilevel inverter and shows the principle of constructing an input line voltage through two components and , obtained when the multilevel inverter, in this case operating on five levels.
The proposed converter allows the improvement of the input line voltage by reducing its THD. It is important to notice that, only a fraction of the total output power is required to flow through the converter parallel circuits, supporting a competitive economic impact. It was experimentally observed that for the multilevel inverter operating as a inverter, just about 20% of the total output power is processed by the parallel inverter and a less than 14% in the input line voltage can be achieved. Besides, one can observe that a variety of harmonic content restrictions imposed by IEEE std 519–1992 can be easily meet by the hybrid inverter presented in this paper, as one can see in Fig. 9. For example, is imposed through the inverter parallel, the input line voltage, will be built of the combination of and with a very low (around 5%). In this case, the converters will supply about 45% of the rated power. Thus, this flexibility is a very good characteristic of the proposed hybrid power inverter system when compared to other multipulse inverter structures.

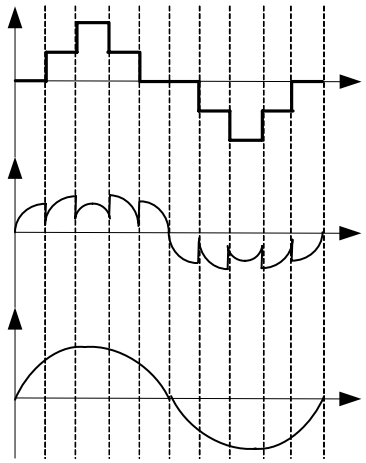

Fig. 9 - Theoretical waveforms for hybrid inverter THD in the input line voltage.

Depending on the kind of application, the proposed hybrid inverter can operate in accordance to the harmonic content restrictions of the input line current with the parallel inverter processing just the minimum power. Therefore, the whole structure presents reduced cost, volume and, higher efficiency when compared to other multilevel inverters. Moreover, the economical benefits of this new topology are extremely valuable for high power installations, because around 33% maximum value of rated power will be processed in the parallel circuits (Proposed Three Level Half Bridge Inverter), in order to reduce the to a very low value (around 5%).
This feature allows higher efficiency and payback in a very short time for the investment. Moreover, when used in retrofitting applications, the available total rated power will increase to 133% of the original output power, with obvious improvements on power quality. In this paper, the authors show the proposed hybrid inverter operating as a conventional five level inverter. The imposition of a sinusoidal input voltage waveform is under progress and will be reported in the future.
It should be emphasized that for isolation to Proposed Three Level Half Bridge Inverter fed through transformers, there is galvanic isolation, as shown in Fig. 10. As a result, such structure is able to replace inverter, but with the obvious drawbacks (volume, weight and cost) of requiring extra magnetic devices. The authors discuss in [20] the implementation higher frequency transformer.

Hence, the control of the Proposed Three Level Half Bridge Inverter current is no longer lost resulting that the desired input line voltage waveform can be achieved. It is important to emphasize that, even using single-phase isolating transformers, the proposed hybrid deploying a inverter with 2 switches to make the complementation of waveform for a sinusoidal output waveform is still more attractive than the multipulse inverter structures presented in [12], [13], [14].

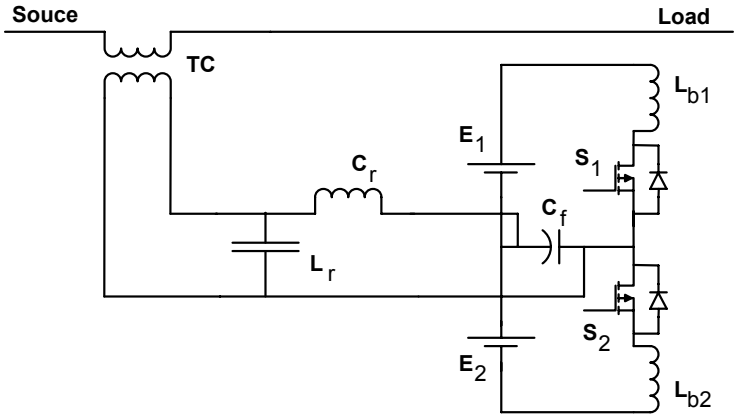

Fig. 10 - New hybrid inverter.

4. PROPOSED CONTROL STRATEGY [15]

The main control circuit objective is to impose the input line voltage at low THD. Therefore, the control strategy must focus on establishing the best relationship between the input voltage of the standard multilevel inverter and the input voltage of the controlled Proposed Three Level Half Bridge Inverter, in order to achieve a desirable input line voltage THD. As example, if a twelve pulses ac current waveform is desired, the control strategy of the controlled proposed inverter can be established as shown in the diagram of Fig. 11.

In order to compose the waveform of the input line voltage, a sample of the input line-to-neutral voltage must be inverted and compared with dc voltage levels in order to generate a synchronized square wave to impose the input half bridge inverter depicted. The voltage is the reference voltage waveform and can be supplied either by analog or digital devices. It was found that, when operating as a conventional five level inverter, the lowest input line current THD is achieved when the magnitude of the voltage is 33% of the magnitude of the principal inverter. Therefore, the reference voltage must be multiplied by a fraction of the current of multilevel inverter providing a reference signal equal to , where k is equal to of the dc current through the output inductor filter of the three-phase five level inverter for the minimum THD .

In order to generate a PWM reference signal, a saw tooth voltage waveform is added to the multiplier circuit signal. Finally, the PWM reference signal must be compared with the cur rent flowing through the Proposed Three Level Half Bridge Inverter to generate the gate-drive signal for switch. Hence, the current through the voltage signal will follow the imposed reference through a very simple PWM control strategy

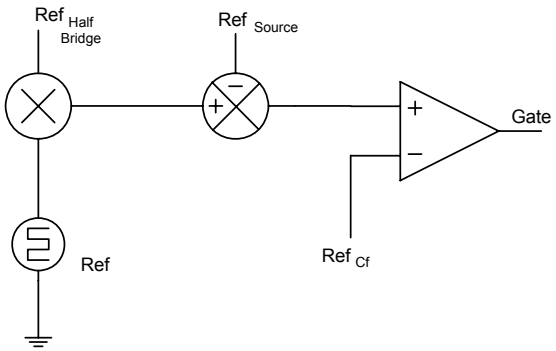

Fig. 11 - Proposed control strategy.

5. RERSULTS

In order to analyze the operation of the proposed Hybrid Inverter, a digital simulation was performed and then compared with experimental results. Table I shows the system specifications. A multilevel inverter control strategy was applied in order to control the proposed structure, waveform in the line input voltage. Thus, the proposed control shown in **Fig. 10** was implemented, and used for simulation analysis. An open loop control strategy, following the principles depicted in Fig. 6 was implemented in power electronics simulation software.

The simulation results for the input line voltage composition are portrayed in **Fig. 12** and **Fig. 13**. **Fig. 12** shows the input current from the controlled Proposed Half Bridge, considering highly dc inductive filters.

Fig. 14 shows the simulation of input voltage and voltage waveforms where it can be observed that multilevel inverter input voltage waveform was imposed in the input line current, resulting in a THD near to 13.7%, for nominal output power. **Fig. 15** shows the frequency spectrum of the input line current, for rated load. The ripple voltage over the average nominal output voltage is depicted on **Fig. 16**.

The simulation studies supported the best relationship between the magnitudes of current magnitude and current to be about 33%. This relationship gives the lowest of 13.55% for a multilevel inverter waveform in the line input voltage, as shown in **Fig. 15** shows the power rating of Proposed Three Level Half Bridge Inverter in relation to the total output power. Therefore, one can observe that, processing only 15.29% of the total output power, less than 14% of THD in the line input current is achieved.

Table 1: Designed parameters and used semiconductors

Data Specifications	
Total Output Power = 1.0 kW	
Multipulse Inverter	**Three Level Associated Inverter**
Input Voltage = 150V	Input Symmetrical Voltage = 150V
Output Voltage = 127V $_{RMS}$	Output Voltage = 127V $_{RMS}$
Output Power = 850W	Output Power = 150W
Switches = IRFP460	Switches = IRFP460
Diodes = HF15TB60	Diodes = HF15TB60
	Inductor (Lb) = 400µH
	Capacitor (Cf) = 15µF

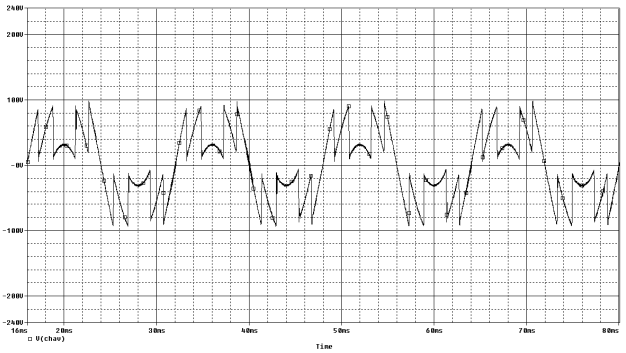

Fig. 12 - Input voltage Proposed Three Level Half Bridge Inverter.

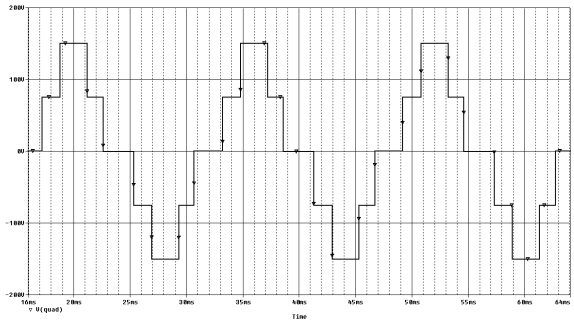

Fig. 13 - Input voltage multilevel inverter.

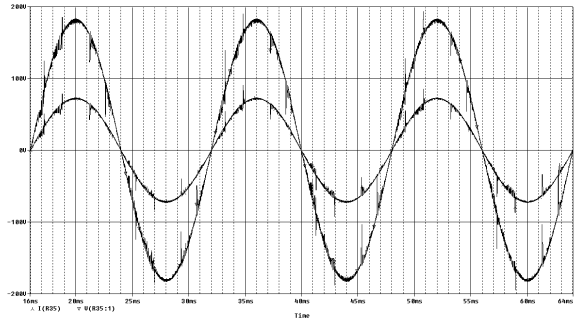

Fig. 14 - Sinusoidal input voltage waveform of Proposed Hybrid Inverter

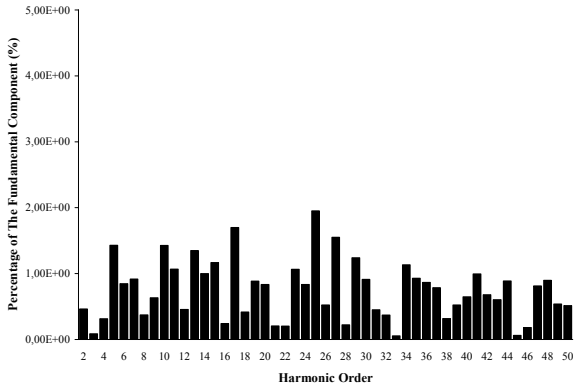

Fig. 15 - Frequency spectrum of the output line voltage.

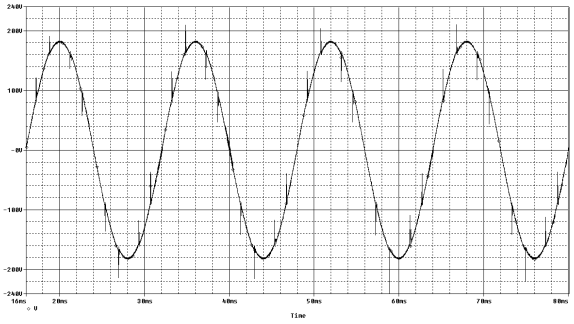

Fig. 16 - Output voltage.

6. CONCLUSION

This paper introduced a novel three-phase hybrid power inverter capable of achieving nearly unity output distortion with programmable input line voltage THD. The paper presented comprehensive analysis, evaluation and design of a system composed of single-phase Half Bridge Inverter connected to each leg of a standard uncontrolled three-phase six-pulse diode rectifier. The parallel converters power rating is only a small fraction of the total output power supporting a competitive economic impact.

Additional analyses were presented to determine the amount of power processed by the controlled rectifiers, in order to obtain a given (and desirable) total harmonic distortion in the input line voltage . It was verified that for less than 15% only 21% of the rated output power had to be processed by the Half Bridge Inverter. Therefore, this proposed structure is recommended for high power installations, and retrofitting to existing installations is feasible since the parallel path can be easily controlled by integration with the existing dc-link. The proposed structure provided a multipulse ac input voltage with simplified design and reduced cost. In addition to the converter analysis and simulation results, experimental results from a 1 kW simulation project were presented, in order to validate the proposed structure and control strategy. The author is working on further developments towards a fully digital programmable control (using DSP and FPGA devices) for the proposed converter

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REFERENCES

[1]. J. S. Lai and F. Z. Peng, "Multilevel converters–A new breed of power converters," IEEE Trans. Ind. Applicat., vol. 32, pp. 509–517, May/June 1996.

[2]. L. Tolbert, F.-Z. Peng, and T. Habetler, "Multilevel converters for large electric drives," IEEE Trans. Ind. Applicat., vol. 35, pp. 36–44, Jan./Feb. 1999.

[3]. R. Teodorescu, F. Beaabjerg, J. K. Pedersen, E. Cengelci, S. Sulistijo, B. Woo, and P. Enjeti, "Multilevel converters — A survey," in Proc. European Power Electronics Conf. (EPE'99), Lausanne, Switzerland, 1999, CD-ROM.

[4]. J. Rodríguez, F. Z. Peng and J. S. Lai "Multilevel Inverters: A Survey of Topologies, Controls, and Applications" IEEE Transactions on Industrial Electronics, vol. 49, no. 4, august 2002, pp. 724-738

[5]. J. S. Lai and F. Z. Peng, "Multilevel converters–A new breed of power converters," IEEE Trans. Ind. Applicat., vol. 32, pp. 509–517, May/June 1996.

[6]. T. A. Meynard and H. Foch, "Multi-level choppers for high voltage applications," Eur. Power Electron. Drives J., vol. 2, no. 1, p. 41, Mar. 1992.

[7]. C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison multilevel inverters for static var compensation," in Conf. Rec. IEEE-IAS Annu. Meeting, Oct. 1994, pp. 921–928.

[8]. P. Hammond, "A new approach to enhance power quality for medium voltage ac drives," IEEE Trans. Ind. Applicat., vol. 33, pp. 202–208, Jan./Feb. 1997.

[9]. E. Cengelci, S. U. Sulistijo, B. O. Woom, P. Enjeti, R. Teodorescu, and F. Blaabjerge, "A new medium voltage PWM inverter topology for adjustable speed drives," in Conf. Rec. IEEE-IAS Annu. Meeting, St. Louis, MO, Oct. 1998, pp. 1416–1423.

[10]. R. H. Baker and L. H. Bannister, "Electric power converter," U.S. Patent 3 867 643, Feb. 1975.

[11]. R. H. Baker, "Switching circuit," U.S. Patent 4 210 826, July 1980.

[12]. S. Martinius, B. Halimi, and P. A. Dahono, "A transformer connection for multipulse rectifier applications," in Proc. Power Syst. Technol. (POWERCON'02), 2002, pp. 1021–1024.

[13]. J. Hahn and P. N. Enjeti, "A wide input range active multi-pulse three-phase rectifier for utility interface of power electronics converters," in Proc. IEEE-Ind. Appl. Soc. Annu. Meeting (IAS'02), 2002, pp. 2514–2519.

[14]. L. C. Gomes de Freitas, E. A. A. Coelho, A. P. Finazzi, M. G. Simoes, C. A. Canesin, and L. C. de Freitas, "Programmable PFC based hybrid multipulse power rectifier for utility interface of power electronic converters," in Proc. IEEE Power Electron. Spec. Conf. (PESC'05), 2005, pp. 2237–2243.

[15]. Carlos A. Gallo, Vladimir V. R. Scarpa, Fábio R. Vincenzi, Fernando L. Tofoli, Ernane A. A. Coelho, Luiz Carlos de Freitas, Valdeir J. Farias, João Batista Vieira Jr. "A New Topology of Three-Level Half Bridge Inverter", IEEE Power Electronics Specialists Conference (PESC'04), 2004, pp. 3873–3876.